SPEKTROP DPU: Opto-electronic platform for fast multi-spectral imaging

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ABSTRACT

In recent years it is easy to spot an increasing need for high-quality Earth imaging in airborne and space applications. This is due to the fact that government and local authorities urge for up-to-date topological data for administrative purposes. On the other hand, interest in environmental sciences, push for ecological approach, efficient agriculture and forests management are also heavily supported by Earth images in various resolutions and spectral ranges.
"SPEKTROP DPU: Opto-electronic platform for fast multi-spectral imaging" paper describes architectural details of data processing unit, part of universal and modular platform that provides high quality imaging functionality in aerospace applications.

Keywords: SPEKTROP, FPGA, SATA, Ethernet, gigabit serial communication, camera, Earth imaging

1. INTRODUCTION

SPEKTROP is a research and development program, run by Space Research Center of the Polish Academy of Sciences. Its main goal is to create a prototype of spectrometer for analyzing electromagnetic spectrum in the wavelength range from 300nm up to 18μm, with the highest detector (image sensor) resolution 2000x4000 pixels. Applications covered by SPEKTROP are Earth observation for satellites and unmanned aerial vehicles. It involves research in many areas, including fast data processing platform, vibration mitigation and novel approach for optics design. The key design drivers in SPEKTROP are the system modularity allowing easy customization for specific realization constraints and scalability allowing use of various image sensors. All components are carefully chosen, in a way that let SPEKTROP be airborne or space system, without need of major modifications.
SPEKTROP DPU (Digital Processing Unit) is a heart of a system that pumps the imaging data from analog, optoelectronic part, processes the data accordingly and stores it in mass memory or forwards to the end-user through broadband access interface. Additionally, all housekeeping and maintenance activities, clock generation and user interfaces are provided by DPU, as well as detachable high data throughput mass memory block.
Therefore there can be four main functional blocks outlined in DPU: analog part (with image sensor, power conversion electronics and analog to digital converters), data acquisition part, processing, command and housekeeping part (user interface, image processing algorithms, broadband interface) and mass memory part (RAID0 matrix build on several solid state drives). All data processing and user interface activities are realized by FPGAs of Virtex 5 family with vast logic resources and peripherals.

2. DESIGN CONCEPT

Presented paper describes design details implemented in SPEKTROP DPU, that makes this platform a novel approach to aerospace data processing systems. One of key design drivers of presented DPU is to ensure large data throughputs on input and output of the system (theoretically, frame rates taken into account are between 50 and 500 frames per second), as well as circulate and process the data efficiently inside the system. Therefore, where possible, very high speed serial interface are implemented to keep EMI, harness and mass on reasonable level.
Additionally, steps are taken to keep analog unit physically separated from acquisition and processing unit. Analog part, kept separately is isolated from digital noise and, if necessary, can be attached to attitude control and vibration attenuation modules. Analog signals (as well as some clock and control signals) are differentially transmitted to main unit where they are sampled and processed further. Several architectures of DPU were under analysis. They can be divided in two classes. One class (class 1) is built around using one large FPGA with around 40 serial ports. Second class (class 2) of architectures is built around multi FPGA approach, where some chips data acquisition, processing, all communication tasks are spread over 2 or 3 chips. Table 1 contains trade-off analysis of 3 examples taken into account.

#	Architecture	Complexity	Features	Cost
1	1 * 150TXT (*class 1*)	1	2	2.5
2	3 * FX30T + 1 * FX70T (*class 2*)	3	2	1.9
3	2 * SX50T + 1 * FX70T (*class 2*)	3	3	2.9

Table 1. Trade-off analysis of possible SPEKTROP PDU architectures

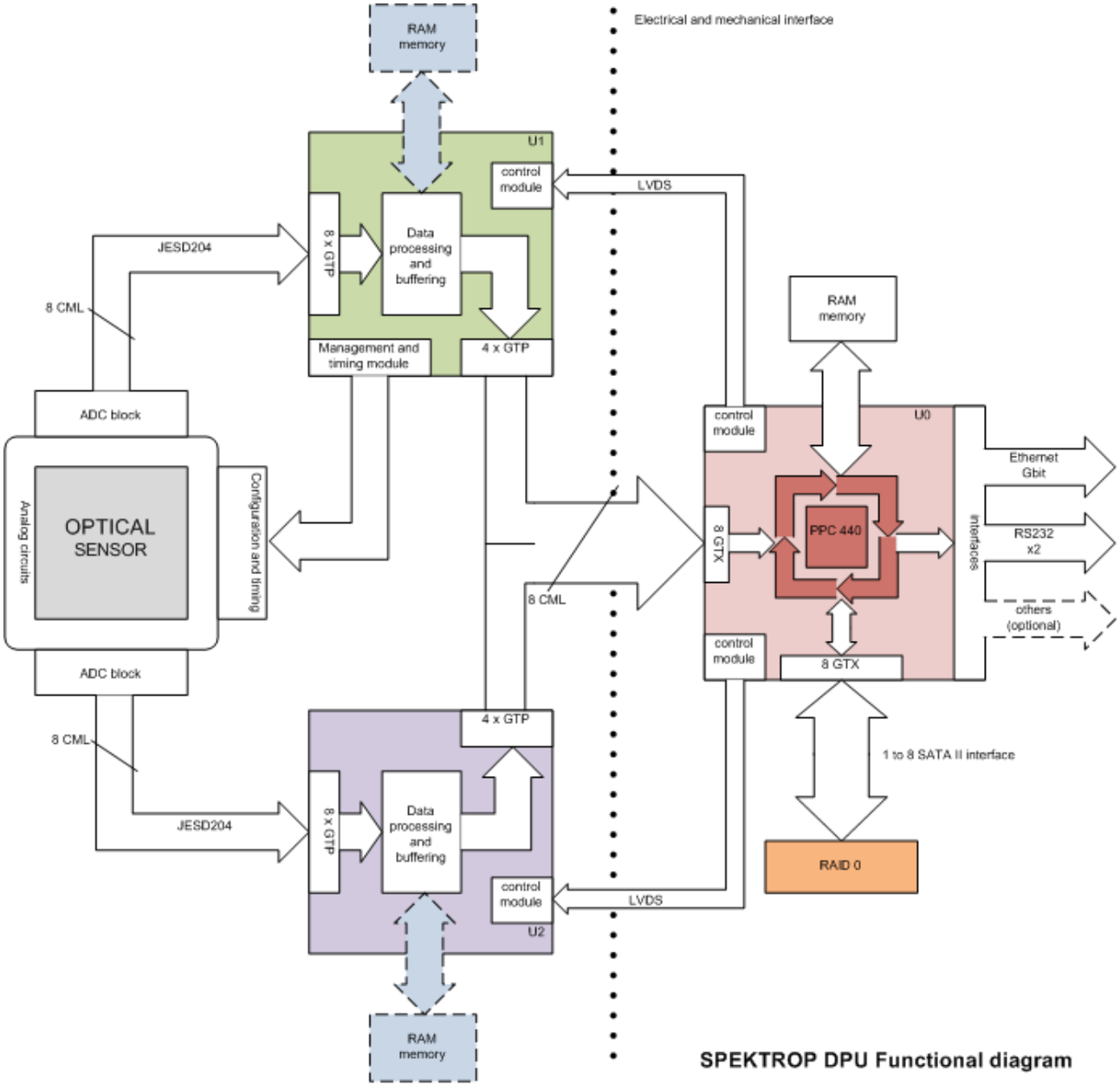

Figure 1. Functional block diagram of desired DPU architecture

Analysis summed up in Table 1 needs explanations. Architecture defines proposed Virtex 5 FPGAs – type and number of chips. FXT devices are perfect for embedded systems, SXT contain additional DSP resources, LXT are just ordinary

Virtex 5 chips where TXT are chips with enormous serial communication resources. Complexity, on a scale from 1 to 3, where 1 is easiest, considered how much effort is needed to design a PCB, interconnect all parts of design. Features, on a scale from 1 to 3 where 1 is least rich in features, considered how much of the whole DPU concept will be proven. Cost, in thousands of Euros, is an estimated cost of the most important chips.
Two out of three presented architectures were grayed out – means they were chosen as good options. As an outcome of the study it became clear that most desirable is architecture 3 as it is most flexible in terms of possible modifications and has a lot of valuable resources (depicted on Figure 1). On the other hand, for demonstration purposes, architecture number 1 seems to be good option, as one chip makes it fairly easy to implement and all features can be explored and technologies tested, except for inter-chip communication, which is not the most important issue at the moment [1].

3. TECHNOLOGY DEMONSTRATOR

One of goals of the SPEKTROP project is to build a technology demonstrator. As technology demonstrator is more constrained than the general design concept, several decisions with trade-off analyses were taken to ensure that the demonstrator proves the functionality and performance is feasible to be achieved in a given budget and time limits. In the first turn, functional blocks are implemented (to a possible extent) in ML507 development boards. In the second phase, a custom board will be designed.

3.1 Image sensor

According to the project goals there was a decision to use set of three different detectors. First detector was chosen for high speed analyzes, up to 500fps, in the visual range from 300nm up to 900nm and the resolution of 512x512. The second detector was chosen for testing the CCD-TDI technology. This detector is a high speed matrix, reading up to 50000 lines per second, sensitive in visual range from 200nm up to 1000nm .The third detector was chosen for long wave infrared (LWIR) analyzes. The detector gives a possibility to analyze spectrum from 8μm up to 14μm with the resolution of 384x288 pixels. With presented detectors the following techniques can be verified: creating a spectrometer analyzing visual and infrared spectrum, working with CCD[1], CCD-TDI[2] and bolometer detectors, working with ultrafast detector up to 30Mpps, constructing 16 channels high speed analogue electronics, creating calibration algorithms for visual and infrared spectrum analyzes.

3.2 Sensor readout circuits

In most designs the DC level is removed from signal just after detector output. The video signal can be easier gained but additional DC level restoration noise is added to the signal. The idea is to acquire video signal together with DC level, which is possible only for low DC level and for low gain of the first stage of the amplifier. For one of the detectors the DC level is 5V and the video signal amplitude on the detector output is ~400mV, which makes it ideal for proving a proposed solution. In the first step the gain of LNA[3] was set to x2 which gives video signal amplitude ~800mV on the 10V DC level. The chosen ADC converter has 1.25V input voltage range, which means that after LNA the signal should be two times larger. The following formulas theoretically show improvement introduced by the presented idea. (1) and (2) represent video signal noise after analogue chain for standard and modified design, (3) estimates the value of improvement:

$$N_{tot1} = \left(\left(N_{\det} + N_{LNA} + N_{DCrest}\right) * G_{LNA} + N_{OpAmp2}\right) * G_{OpAmp2} \quad (1)$$

$$N_{tot2} = \left(\left(N_{\det} + N_{LNA}\right) * G_{LNA} + N_{OpAmp2} + N_{DCrest}\right) * G_{OpAmp2} \quad (2)$$

$$\Delta N_{tot} = N_{DCrest} * G_{LNA} * G_{OpAmp2} - N_{DCrest} * G_{OpAmp2} = N_{DCrest} * G_{OpAmp2} * \left(G_{LNA} - 1\right) \quad (3)$$

where:

$N_{\det}$	- the detector video signal noise	G_{LNA}	- the first stage amplifier gain
N_{LNA}	- the first stage amplifier noise	G_{OpAmp2}	- the second stage amplifier gain
N_{DCrest}	- the DC restoring circuit noise	N_{OpAmp2}	- the second stage amplifier noise

[1] CCD – Charge Coupled Device
[2] CCD-TDI - Charge Coupled Device Time Delayed Integration
[3] LNA – Low Noise Amplifier

3.3 Noise immunity

The second idea is to use fully differential analogue chain for delivering video signal to ADC converter. The advantages of such solution should be:

- increasing the video signal immunity against internal and external distortion
- increasing physical distance between last operation amplifier and ADC converter without decreasing analogue signal quality
- increasing the detector thermal decoupling from high power dissipation elements

The schematic of the proposed idea is presented in Figure 2. The video signal from the detector will be amplified by the first stage of LNA, afterwards a single-ended signal will be transformed on a fully differential signal. The differential lines will transport a fully differential video signal to ADC input. The test signal plots for characteristic points, showing an idea of the presented differential chain, are shown in Figure 3 and 4. On Figure 3, the first signal "1" represents a video signal on the detector output that was generated by an external function generator. The second signal "2" represents video signal after the first stage of amplifier, the higher level of signal can be observed. The "3" and "4" signals represent video signal on the output of a fully differential amplifier. The scope gain for the signal "1" is set to 1V/div and DC coupled, for the signal "2" is set to 2V/div and DC coupled, for signal "3" and "4" is set to 1V/div and AC coupled.

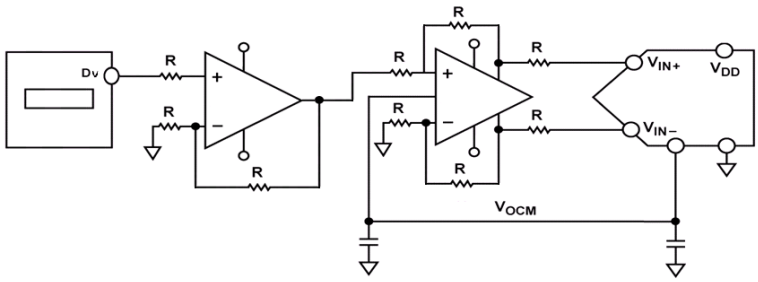

Figure 2. The schema of fully differential analogue chain.

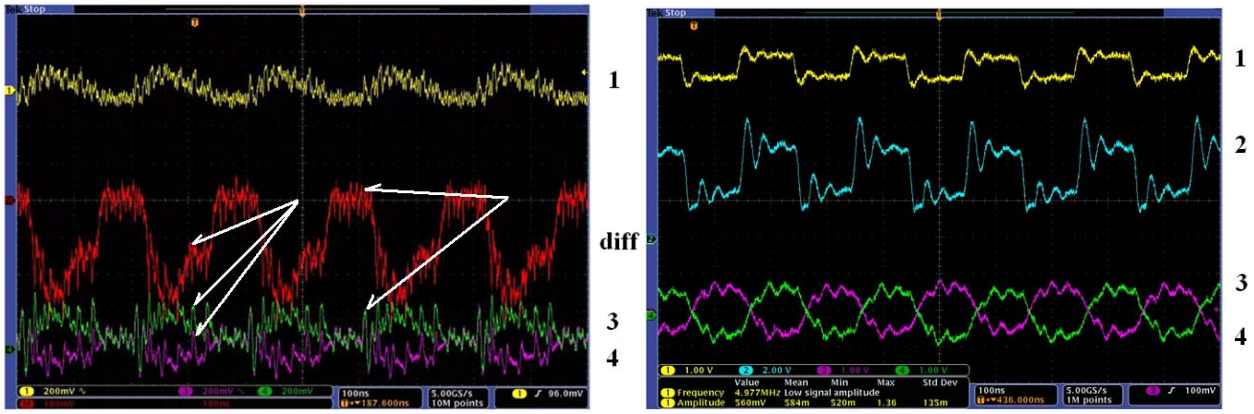

Figure 3 and 4. The test signal plots from characteristic points of the analogue chain.

Figure 4 shows the weak video signal from the detector in characteristic points of the analogue chain. The first signal "1" shows a video signal on the detector output, for short exposition time. The "3" and "4" signals represent video signal on the output of a fully differential amplifier. By using the scope match function, the differential representation of video signal is generated in the form of the "diff" signal. The scope gain for all signals is set to 200mV/div AC coupled, the gain for math function, is set to 100mV. The arrows show points where the advantage of fully differential chain can be observed. The high amplitude disturbance from power lines and timing generator visible on differential signals are almost completely removed from the differential signal.

3.4 Data input

Demonstrator model of SPEKTROP DPU receives data from up to 16 ADCs, at maximum bit rate of 1.9 Gb/s which leads to 3.8 GB/s of total input data stream. As gathered data is not only pixel value, but dark and reset values, and the whole stream is encoded in 8b/10b scheme, then estimated raw data stream is around 1.5GB/s, which is around 50% more than predicted maximal throughput of mass memory. In fact this is not a problem, as image sensors connected to the system are much slower than the highest ADC sampling rate used in calculations. Highest, raw data rate expected in the experiment, is 280 MB/s.

3.5 Serial data transmission

One of key solutions implemented in DPU is high speed serial data transmission. It is presented in two areas. One, is the communication between ADCs and the other is communication with solid state mass memories. Both solutions, use alike GTX RocketIO (up to 6.5 Gb/s) ports that define physical layer for data exchange. It is worth noticing that such communication uses 8b/10b (sometimes 64b/66b) encoding scheme to ensure enough number of zeroes and ones in the data stream. Hence, the data stream can pass AC coupled channels (in average, coupling capacitances are not charged) and due to sufficient number of edges in data stream, bit clock can be recovered. Recovering clock from the data stream is a very handy technique that simplifies clocking of the whole system – recovered clock is always in phase with incoming, serialized and parallel data. Linear LT2272/3 ADCs generate the data stream at 65 and 85 MSa/s respectively, which relates up to 1.9 Gb/s bit rate. This is more than enough for image sensors that are going to be tested with DPU, and uses below 30 percent of GTX RocketIO maximum speed. In turn, SATAII interface for connecting mass memory flash drives, utilizes similar transmission medium, however in larger extent – 3Gb/s [2,3,4].

3.6 Protocol offload engine

Ethernet is the main interface for a user to gather real-time imaging data or to retrieve data stored in the mass memory system. DPU is designed in a way such that it can operate all three standard data rates – 10, 100, 100 Mb/s but it is encouraging, that especially during real time pictures / video streaming, a highest operation speed is used – no data jams and data loss shall occur then. Unlike in a large part of existing designs, Ethernet communication, and whole process of data encapsulation in various Internet protocols is not done by on-board processor (or on-chip processor) but by a efficient custom made and tailored finite state machine – a Protocol Offload Engine, POE. POE manages and drives all on-chip processes that relate to Ethernet and local network communications, including ARP service for MAC address identification, ICMP service for echo requests, UDP / IP for data exchange including observation data, telemetry, commands and batch configuration scripts. POE sequentially reads the data FIFO, and, in parallel feeds the Ethernet FIFO creating Ethernet packet at runtime. Delays and congestions in the data stream are minimal and only due to packet and protocol headers. In the same time, commands received from the local network are decoded and prepared for execution.

Such approach is not the simplest, in terms of time and effort, but resulting data throughput is close to limits defined by the Ethernet interface itself.

3.7 Mass memory

As SPEKTROP DPU is intended for space and airborne applications, it is critical (especially for the latter) to reduce mass and moving mechanisms as much as possible (not mentioning power and heat issues). Mass reduction is a rationale behind a decision of using Flash disks as mass memory. Mentioned disks, have to be connected in parallel in RAID 0 matrix, to raise storage system throughput, to meet requirements imposed by large and fast data input to the system. Baseline disk for demonstrator experiments is the Torqx Patriot Extreme. Used Torqx disks have a volume of 128 GB and (measured) write speed of around 150 MB/s (read speed, measure as well, is 210MB/s but it is not a crucial parameter). As memory system is designed to operate with up to 8 disks, expected write speed is to be around 1 – 1.2 GB/s. In order to achieve described functionality, a custom made RADI0 SATA II controller is developed. It's simple purpose is to divide data stream into narrower substreams and tag data segments accordingly so reconstruction of original stream is possible during read operations. Figure 5 depicts architecture of designed RAID 0 controller. Red is a write stream and green is a read stream. Additionally arrows hold information of the stream direction. Obviously, since SATA is a serial interface, every substream is drained by a RocketIO port serializing/deserializing data and encoding it accordingly within 8b/10b scheme [3].

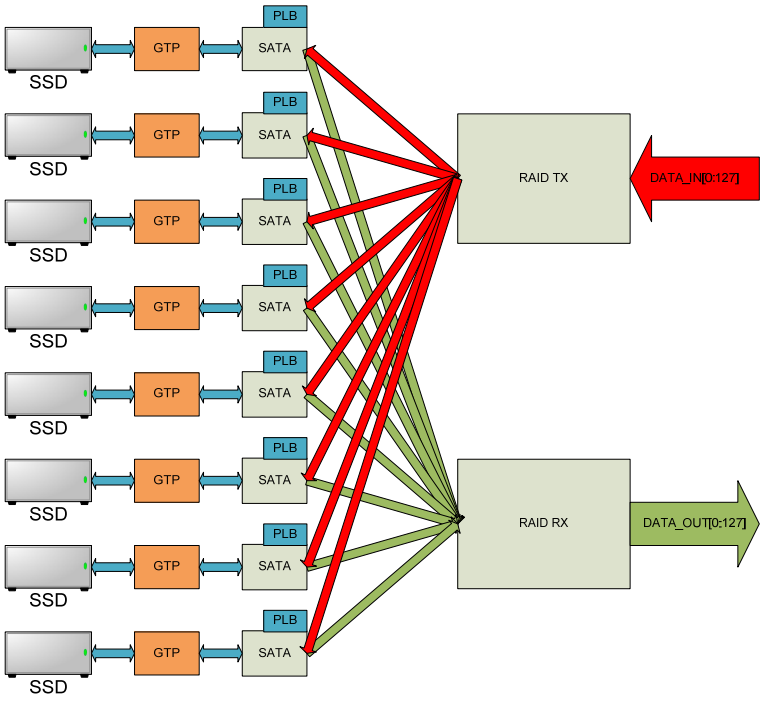

Figure 5. Eight lane SATA RAID0 controller

3.8 Data path modularity

It is clear that, both input and output of DPU (hence, the FPGA) are serial. Therefore, most natural way of designing all on-chip interfaces, processing blocks and transmission interconnects is to keep serial and sequential character of data – keep the data as a stream. Such stream is then leaded from one processing unit to another processing unit through specific troughs – FIFOs. SPEKTROP DPU utilizes two types of FIFOs. One is a primitive RAM block that can be instantiated as FIFO – which is a fast and efficient way of connecting simple blocks. If more sophisticated solution is needed, with handshake support for protocol transmission – LocalLink FIFO is instantiated. An important feature of both examples is the ability to cross different clock domains – therefore acting as instant cache. With both FIFOs defined as interface among processing blocks, high and flexible data path modularity is achieved (Figure 6).

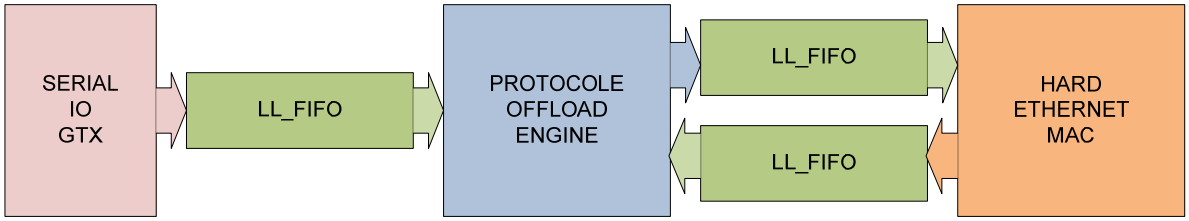

Figure 6. Example data path implemented in early SPEKTROP DPU models

4. SUMMARY

"SPEKTROP DPU: Opto-electronic platform for fast multi-spectral imaging" paper describes novel architecture proposed for aerospace data processing systems which combine high performance, scalability and modularity. Such approach makes them suitable for airborne and space systems without major changes in design.

SPEKTROP DPU demonstrator is a compromise between a vision of an ultra fast, scalable system for data acquisition and processing and a responsibility to prove, step by step, every aspect of technology and concept. It is the first time in the history of Space Research Centre of the Polish Academy of Sciences, that work is carried out on such a wide front of analogue and digital state-of-the-art electronics, so special care is ensured that all basic features, problems and solutions are well understood. It is accepted that in this first step it is more important to build a fully working model of

the SPEKTROP device, having decent parameters, and bringing a lot of new knowledge and experience, than fail by trying to achieve too much at once.

As for the future work the DPU, due to Virtex5 dynamic partial reconfiguration capability, enabling run-time functionality change or adaptive algorithm implementation, may be one of first real designs that implements concept of *morphware*, showing a cutting edge approach to modern computing in high reliability and digital signal processing applications.

5. ACKNOWLEDGMENTS

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